IN THE CLAIMS:

Please cancel claims 1-22 without prejudice and add new claims 23-36. The status of the claims is as follows:

Claims 1-22 (Canceled).

23. (New) A computer system comprising:

an external memory; and

a processor coupled to the external memory, the processor including a replay system to replay instructions which have not executed properly, a first processing circuit coupled to the replay system to process instructions including any replayed instructions based on data in the external memory, a second processing circuit to perform additional processing on an instruction, the second processing circuit having an ability to detect one or more faults occurring therein, and a synchronization circuit coupled between the first processing circuit and the second processing circuit to synchronize faults occurring in the second processing circuit to matching instruction entries in the first processing circuit.

24. (New) The computer system of claim 23, further including an external bus coupled between the external memory and the processor.

25. (New) The computer system of claim 24, wherein the processor further includes an external bus interface coupled to the external bus.

26. (New) The computer system of claim 23, wherein the external memory includes at least one of an external cache memory, a main memory, and a disk memory.

27. (New) The computer system of claim 23, wherein the first processing circuit includes a first event pipeline, and wherein the second processing circuit includes a second event pipeline.

28. (New) A computer system comprising:

an external memory; and

a processor coupled to the external memory, the processor including a replay system to replay instructions which have not executed properly, a synchronous event pipeline coupled to the replay system to process instructions including any replayed instructions based on data in the external memory, an asynchronous event pipeline to perform additional processing on an instruction, the asynchronous event pipeline having an ability to detect one or more asynchronous faults occurring during the additional instruction processing, and a synchronization circuit coupled between the synchronous event pipeline and the asynchronous event pipeline to synchronize an asynchronous fault with a replayed instruction in the synchronous event pipeline.

29. (New) The computer system of claim 28, further including an external bus coupled between the external memory and the processor.

30. (New) The computer system of claim 29, wherein the processor further includes an external bus interface coupled to the external bus.

31. (New) The computer system of claim 28, wherein the external memory includes at least one of an external cache memory, a main memory and a disk memory.

32. (New) The computer system of claim 28, wherein the synchronization circuit includes:

a buffer coupled to the asynchronous event pipeline to store an instruction entry for an instruction having an asynchronous fault, the instruction entry including a sequence number and fault identification information identifying the asynchronous fault; and

a comparator coupled to the buffer and the synchronous event pipeline, the comparator to compare a sequence number of an instruction entry in the synchronous event pipeline with the sequence number of the instruction entry having the asynchronous fault, and to write the fault

identification of the asynchronous fault to the instruction entry in the synchronous event pipeline if a match is found.

33. (New) The computer system of claim 28, wherein the synchronization circuit includes:

an input buffer coupled to the asynchronous event pipeline for store an instruction entry for an instruction having an asynchronous fault, the instruction entry including a sequence number and fault identification information identifying the asynchronous fault;

an asynchronous fault buffer having age guarding logic coupled to the input buffer, the asynchronous fault buffer to store an instruction entry for an instruction having an asynchronous fault in a temporary register; and

a comparator coupled to the asynchronous fault buffer and the synchronous event pipeline, the comparator to compare a sequence number of an instruction entry in the synchronous event pipeline with a sequence number of the instruction entry stored in the temporary register of the asynchronous fault buffer, and to write the fault identification information of the asynchronous fault to the instruction entry in the synchronous event pipeline if a match is found.

34. (New) The computer system of claim 28, wherein the asynchronous fault buffer includes:

age guarding logic coupled to the input buffer; and

a temporary register coupled to the age guarding logic to store an instruction entry for an instruction having an asynchronous fault, the age guarding logic to maintain an oldest instruction entry in the register as compared between an instruction entry having an asynchronous fault already present in the temporary register and an instruction entry for an instruction having an asynchronous fault stored in the input buffer.

35. (New) The computer system of claim 28, wherein the asynchronous fault buffer includes:

age guarding logic coupled to the input buffer;

one or more temporary registers coupled to the age guarding logic to store one or more oldest instruction entries for an instruction having an asynchronous fault, the age guarding logic to maintain an oldest instruction entry in each temporary register as compared between an instruction entry having an asynchronous fault already present in the temporary register and an instruction entry for an instruction having an asynchronous fault stored in the input buffer; and

a mix coupled to the one or more temporary registers to selectively output the instruction entry from a selected temporary register to the comparator.

36. (New) The computer system of claim 35, wherein there is one temporary register provided for each thread or program flow.